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Attorney's Docket No.: 10559-567001  
Client's Ref. No.: P12729**OFFICIAL COMMUNICATION FACSIMILE:****OFFICIAL FAX NO: (703) 872-9306**

Number of pages including this page 5

Applicant : Juan G. Revilla, et al.

Art Unit : 2112

Serial No. : 10/040,904

Examiner : Tim T. Vo

Filed : December 28, 2001

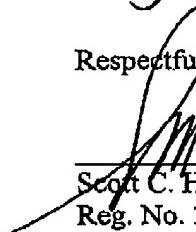
Assignee: Intel Corporation

Title : METHOD AND APPARATUS FOR CONVERTING AN EXTERNAL  
MEMORY ACCESS INTO A LOCAL MEMORY ACCESS IN A PROCESSOR  
CORE

Mail Stop AF  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Attached to this facsimile communication cover sheet are a Response to Office Action  
and Transmittal Letter, faxed this 1<sup>st</sup> day of July, 2005, to  
the United States Patent and Trademark Office.

Respectfully submitted,

Date: July, 2005  
\_\_\_\_\_  
Scott C. Harris  
Reg. No. 32,030  
Attorney for Intel Corporation

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Attorney's Docket No.: 10559-567001 / P12729

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Juan G. Revilla, et al. Art Unit: 2112  
Serial No.: 10/040,904 Examiner: Tim T. Vo  
Filed: December 28, 2001 Assignee: Intel Corporation  
Title : METHOD AND APPARATUS FOR CONVERTING AN EXTERNAL MEMORY  
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TRANSMITTAL LETTER

Correspondence relating to this application is enclosed.  
The required fees are computed below. Please apply any charges  
not covered, or any credits, to Deposit Account No. 06-1050.

|               |    |   |    |   |     |
|---------------|----|---|----|---|-----|
| Total         |    |   |    |   |     |
| Claims        | 33 | - | 33 | = | 0   |
| Independent   | 7  | - | 7  | = | 0   |
| TOTAL FEE DUE |    |   |    |   | \$0 |

Respectfully submitted,

Date: 7/1/05

  
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RESPONSE TO OFFICE ACTION

The following is provided in response to the Office action mailed May 4, 2005.

Reconsideration and allowance of the above-referenced application are respectfully requested.

Allowance of claims 8, 10-14, 22, 24-29, and 33-34 and allowability of claims 2-3 and 16-17 are respectfully noted.

Claims 1, 4-7, 15, 18-21, and 30-32 stand rejected under 35 USC §102. These rejections are respectfully traversed.

Claim 1 recites routing a memory access from a processor core back into the processor core through a bus interface coupled to the processor core without traversing memory external to the processor core. Claims 15 and 30 recite similar limitations.

The Office Action contends that Palanca discloses the features of claim 1 by having a processor core 208 dispatching

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